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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,416	11/16/2001	Ta-Lee Yu	B-4392 619330-6	5531

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EXAMINER

VU, QUANG D

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/992,416

Applicant(s)

YU ET AL.

Examiner

Quang D Vu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 May 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3, 7-12 and 14-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 7-12 and 14-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
- 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
- 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3, 7-12 and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,465,189 to Polgreen et al. in view of US Patent No. 6,071,778 to Bez et al.

Regarding claim 1, Polgreen et al. (figure 8) teach a low voltage triggered electrostatic discharge (LVTESD) protection circuit, coupled to a pad of an integrated circuit to protect core circuits of the IC from ESD event, the ESD protection circuit comprising:

- a semiconductor substrate having the first conductivity type (p-type);
- an well region having the second conductivity type (n-type), formed in the semiconductor substrate;
- an anode doped region having the first conductivity type (p-type), formed in the well region;
- a gate structure (39), formed in the semiconductor substrate and outside the well region, the gate structure (39) having a first side and a second side;
- a first doped region (n-type doped region is on the right side of the gate [39]) having the second conductivity type (n-type), formed between the well region and the gate structure (39),

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immediately adjacent to the first side of the gate structure (39) in the semiconductor substrate;
and

a second doped region (n-type doped region is on the left side of the gate [39]) having the second conductivity type (n-type), formed next to the second side of the gate structure (39) in the semiconductor substrate, wherein the first doped region and the second doped region are heavily doped regions (n+ type).

Polgreen et al. differ from the claimed invention by not showing a plurality of isolated islands distributed in the first doped region so that the resistance of the first doped region is increased, wherein at least one of the isolated islands is completely surrounded by the first doped region. However, Bez et al. (figures 1-6) teach a plurality of isolated islands (65) distributed in the doped region having the second conductivity type (n-type; 6, 7, 14), wherein at least one of the isolated islands is completely surrounded by the first doped region. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Bez et al. into the device taught by Polgreen et al. because it isolates the diffusion areas in the ESD device. The combined device shows a plurality of isolated islands distributed in the first doped region so that the resistance of the first doped region is increased, wherein at least one of the isolated islands is completely surrounded by the first doped region.

Regarding claim 2, Polgreen et al. teach a first contact region (p-type contact region is on the left side of figure 8) having the first conductivity type (p-type), formed in the semiconductor substrate;

a second contact region (n-type contact region is on the right side of figure 8) having the second conductivity type (n-type), formed in the well region; and

the anode doped region (p-type anode region) is coupled to the pad.

Polgreen et al. differ from the claimed invention by not showing the first contact region is coupled to the second doped region and a power pad of the integrated circuit in the embodiment of figure 8. However, Polgreen et al. teach the contact region (p-type; 14) is coupled to the doped region in the embodiment of figure 4. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include claimed limitation shown in the embodiment of figure 4 into the embodiment of figure 8 because it provides interconnection between the contact region and the doped region. The combined device shows the first contact region is coupled to the second doped region and a power pad of the integrated circuit.

Regarding claim 3, Polgreen et al. teach the second contact region (n-type contact region is on the right side of figure 8) is coupled to the anode doped region (p-type anode region).

Regarding claim 7, the combined device shows the isolated islands are field oxide (Bez et al.; 65).

Regarding claim 8, the combined device shows each of the isolated islands (Bez et al.; 65) has approximately the same width.

Regarding claim 9, the combined device shows each of the isolated islands is elongated and approximately parallel to the first side of the gate structure.

Regarding claim 10, the combined device shows each of the isolated islands is elongated and approximately perpendicular to the first side of the gate structure.

Regarding claim 11, Polgreen et al. teach the first conductivity type is a p-type, and the second conductivity type is an n-type.

Regarding claim 12, the disclosures of Polgreen et al. and Bez et al. are discussed as applied to claim 1.

Regarding claim 14, the combined device shows a plurality of oxide layers, and each of the isolated islands (Bez et al.; 65) is formed by one of the oxide layers.

Regarding claim 15, the combined device shows each of the isolated islands (Bez et al.; 65) has approximately the same length.

Regarding claim 16, the combined device shows each of the isolated islands has an elongated profile and is approximately parallel to the first side of the gate structure.

Regarding claim 17, the combined device shows each of the isolated islands has an elongated profile and is approximately perpendicular to the first side of the gate structure.

Regarding claim 18, Polgreen et al. teach the first conductivity type is a p-type, and the second conductivity type is an n-type.

Response to Arguments

Applicant's arguments with respect to claims 1-3, 7-12 and 14-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
May 18, 2004

Sara W Crane
Sara Crane
Primary Examiner